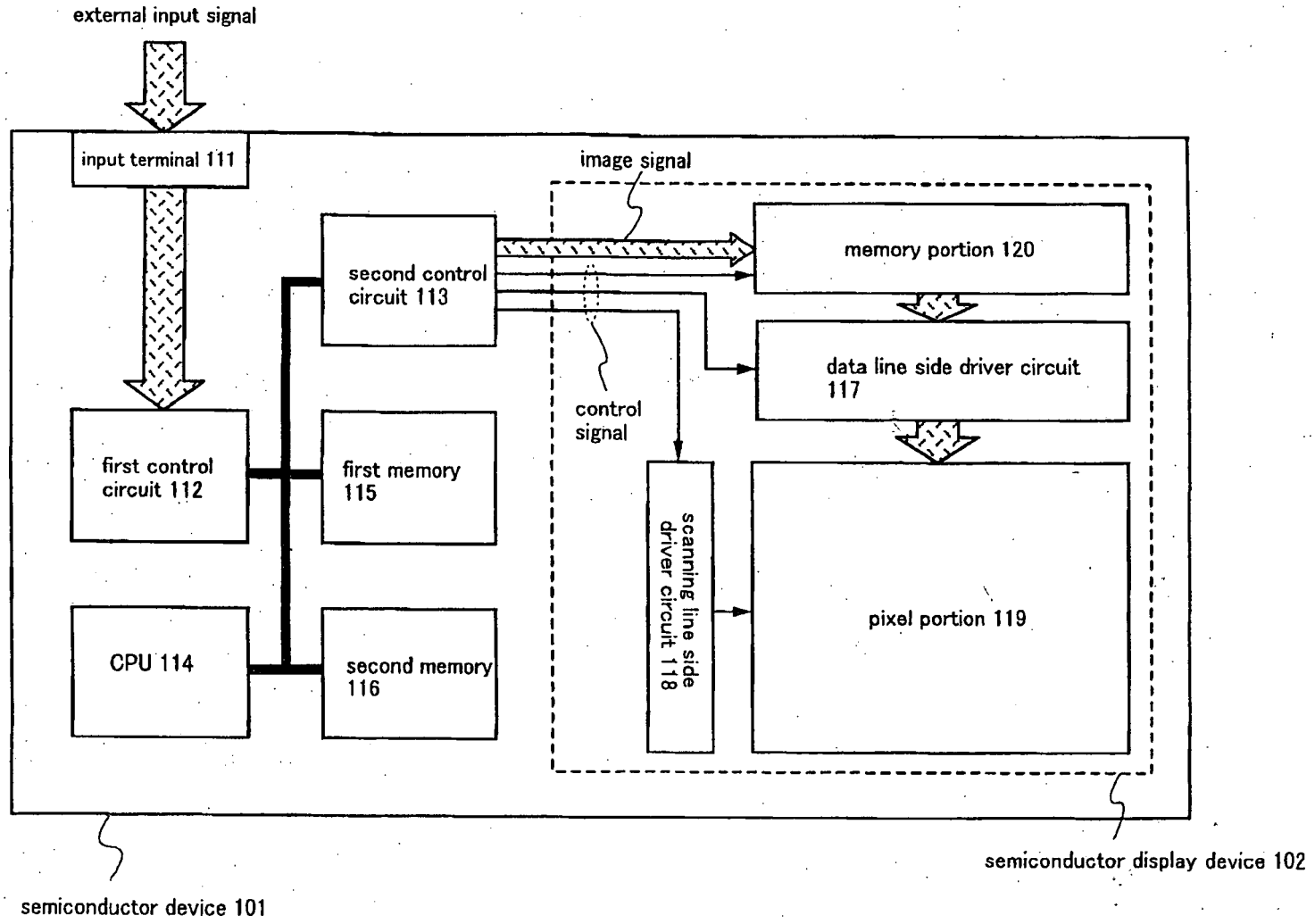
【Fig. 1】


external input signal
input terminal 111
image signal
second control circuit 113
memory portion 120
data line side driver circuit 117
control signal
first control circuit 112
first memory 115
scanning line side driver circuit 118
pixel portion 119
CPU 114
second memory 116
semiconductor device 101
semiconductor display device 102

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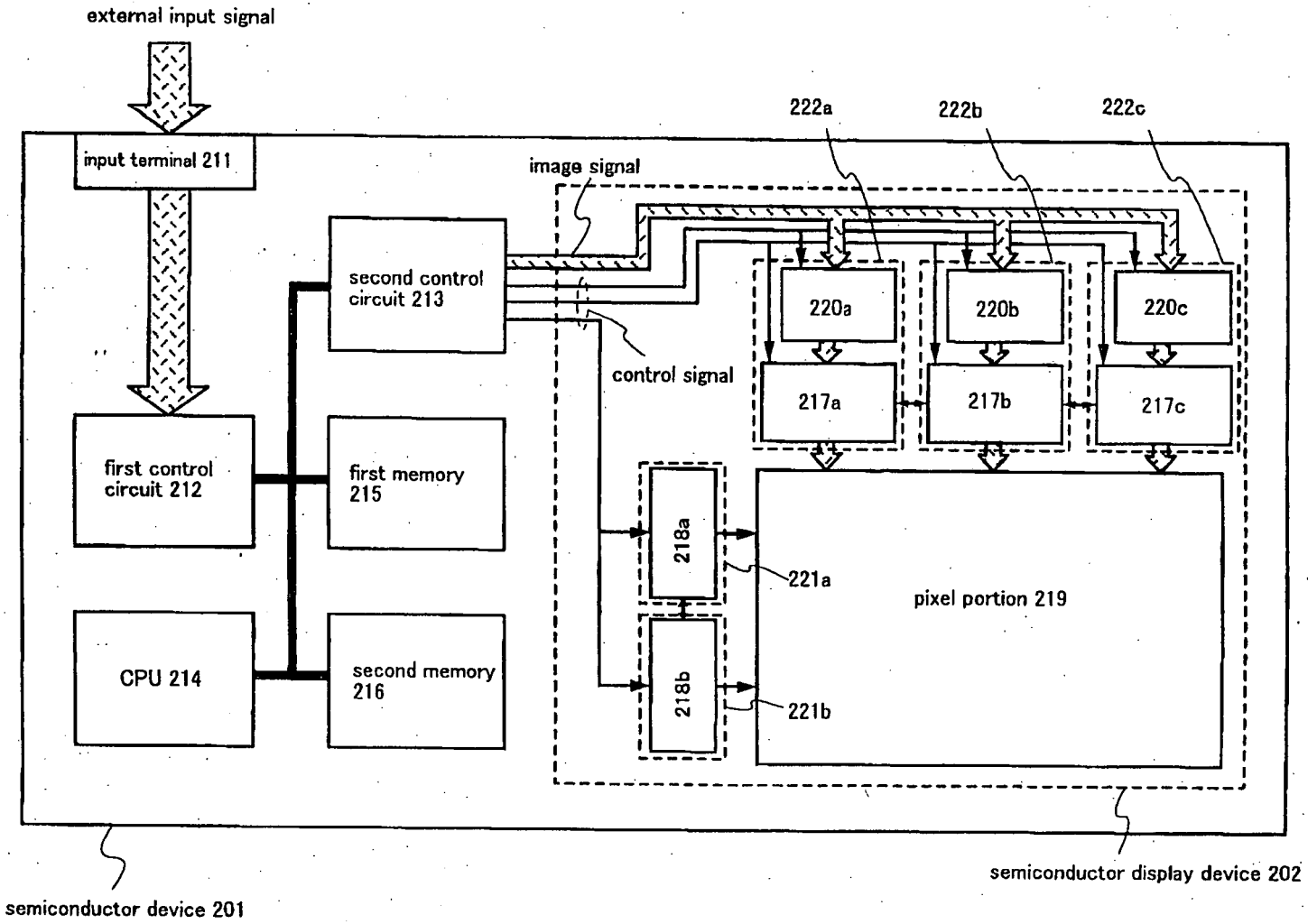
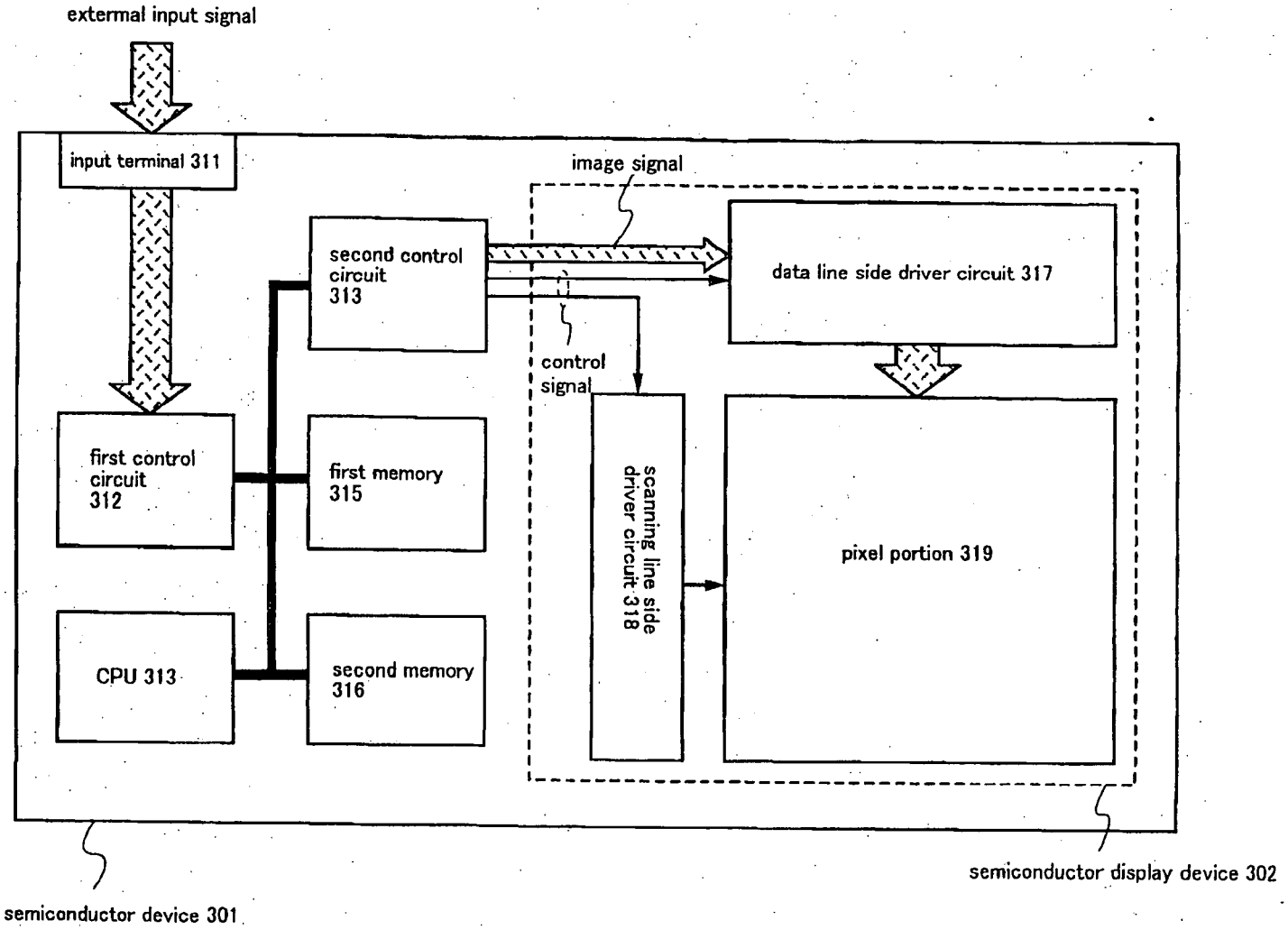
【Fig. 2】



217a, 217b, 217c data line side driver circuit 218a, 218b scanning line side driver circuit
220a, 220b, 220c memory portion 221a, 221b scanning line side stick driver
222a, 222b, 222c data line side stick driver

【Fig. 3】


external input signal
input terminal 311
image signal
second control circuit 313
data line side driver circuit 317
control signal
first control circuit 312
first memory 315
scanning line side driver circuit 318
pixel portion 319
CPU 313
second memory 316
semiconductor device 301
semiconductor display device 302

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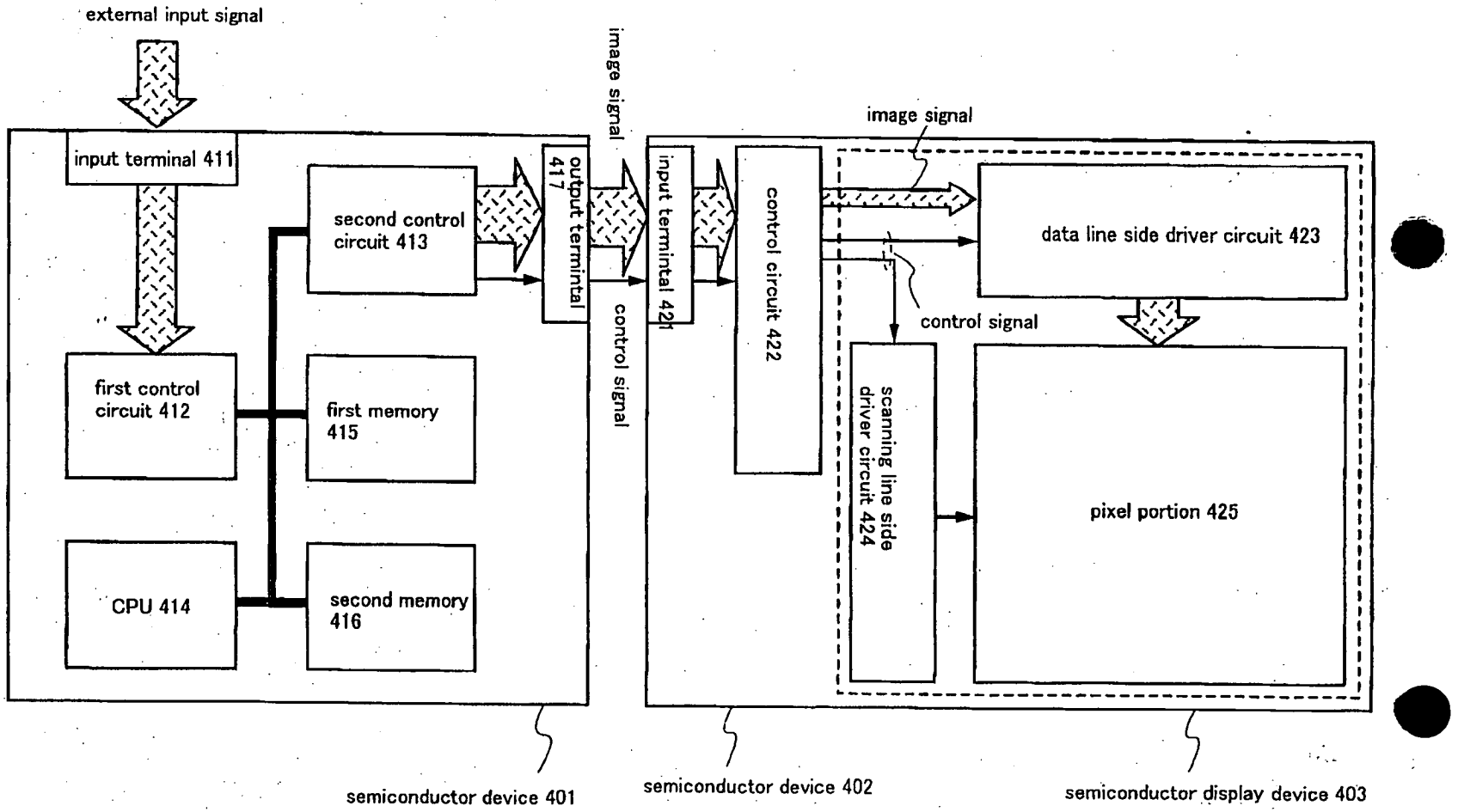
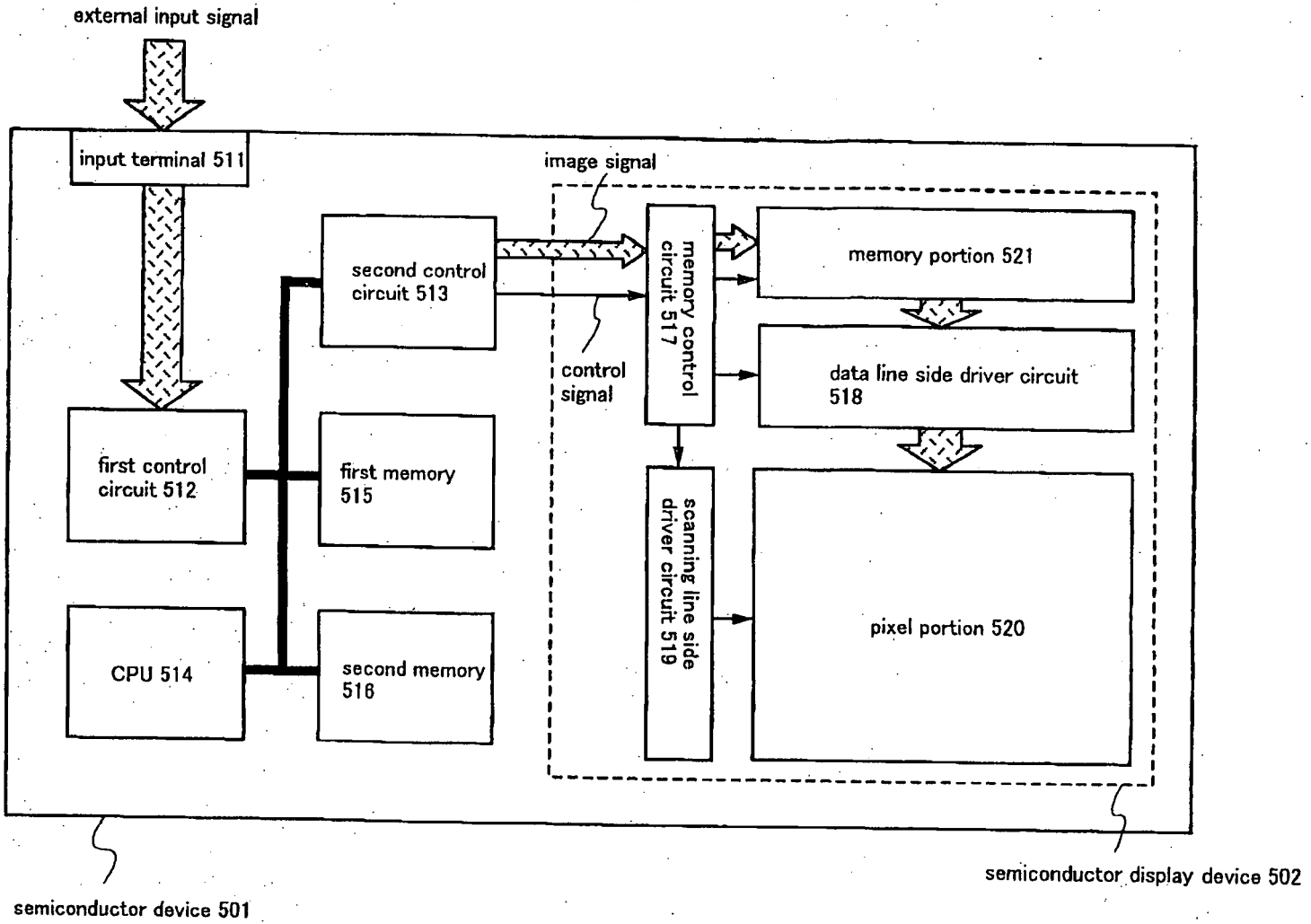
【Fig. 4】



【Fig. 5】


external input signal
input terminal 511
image signal
second control circuit 513
memory control circuit 517
memory portion 521
control signal
data line side driver circuit 518
first control circuit 512
first memory 515
scanning line side driver circuit 519
pixel portion 520
CPU 514
second memory 516
semiconductor device 501
semiconductor display device 502

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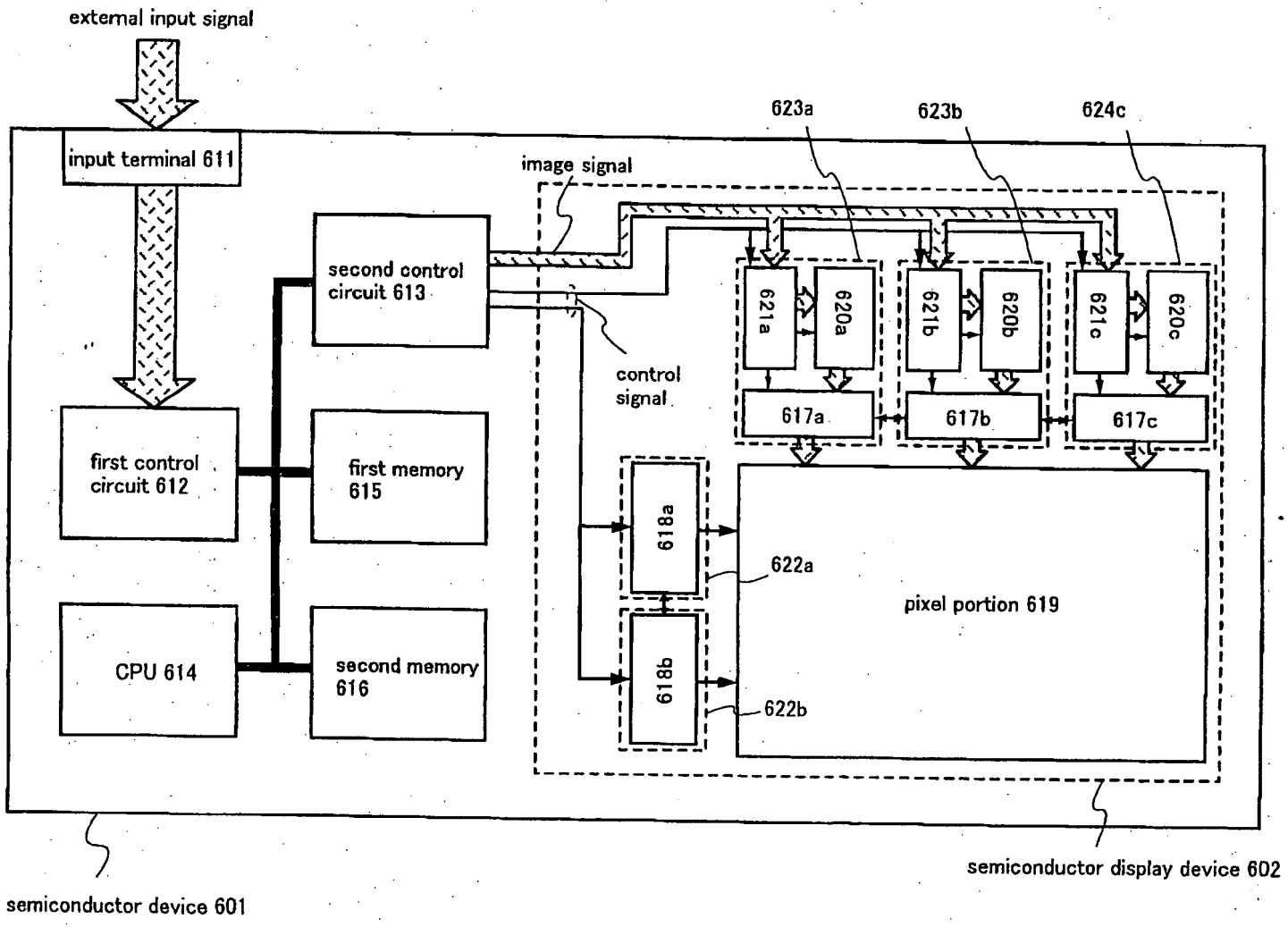
【Fig. 6】



617a, 617b, 617c data line side driver circuit 618a, 618b scanning line side driver circuit
620a, 620b, 620c memory portion 621a, 621b, 621c memory control circuit
622a, 622b scanning line side stick driver 623a, 623b, 623c data line side stick driver

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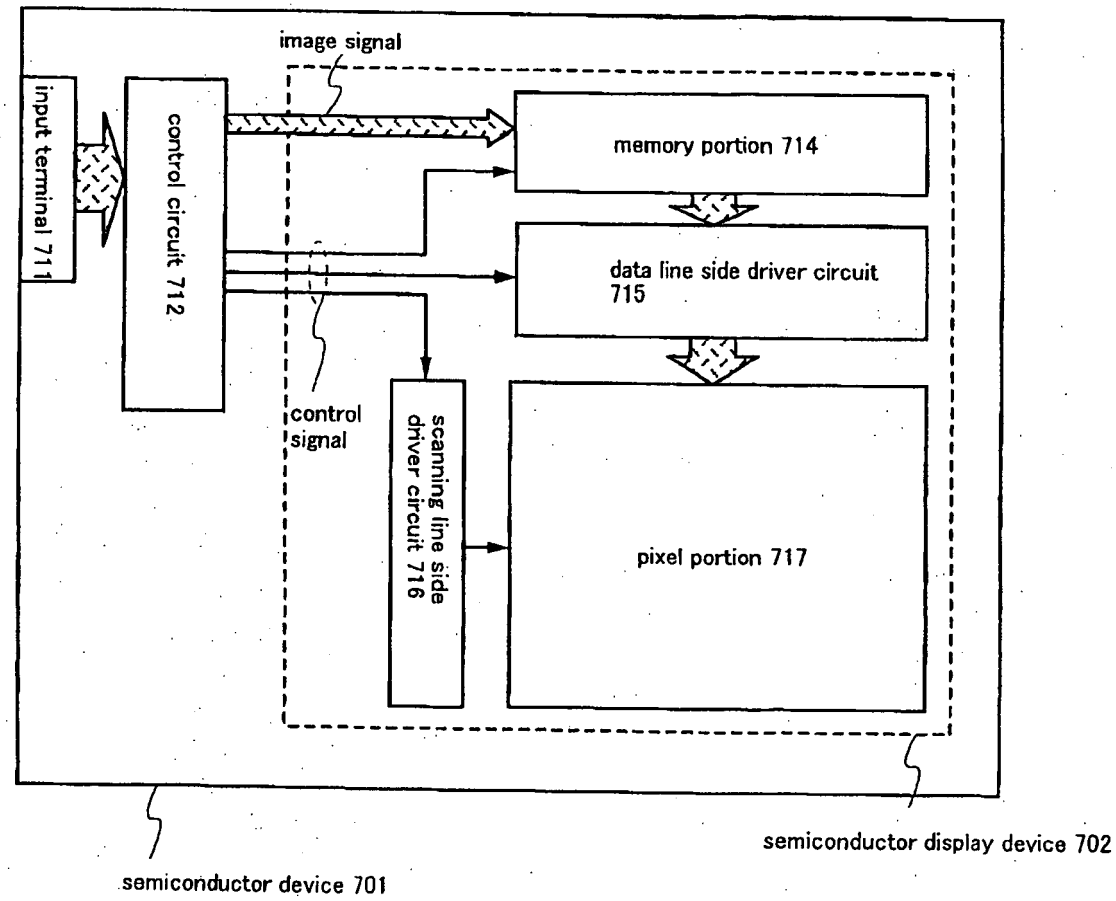
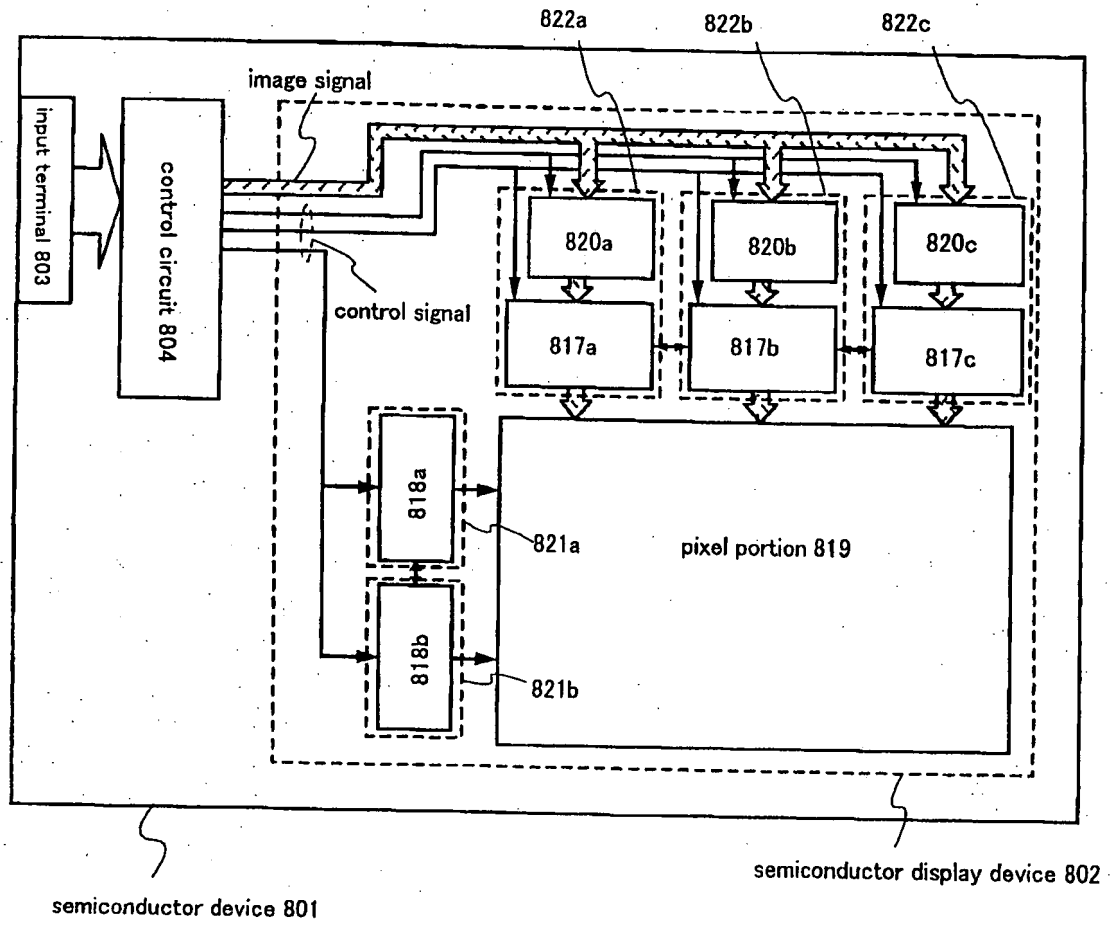
【Fig. 7】



【Fig. 8】



817a, 817b, 817c data line side driver circuit 818a, 818b scanning line side driver circuit
820a, 820b, 820c memory portion 821a, 821b scanning line side stick driver
822a, 822b, 822c data line side stick driver

Fig. 9(A)

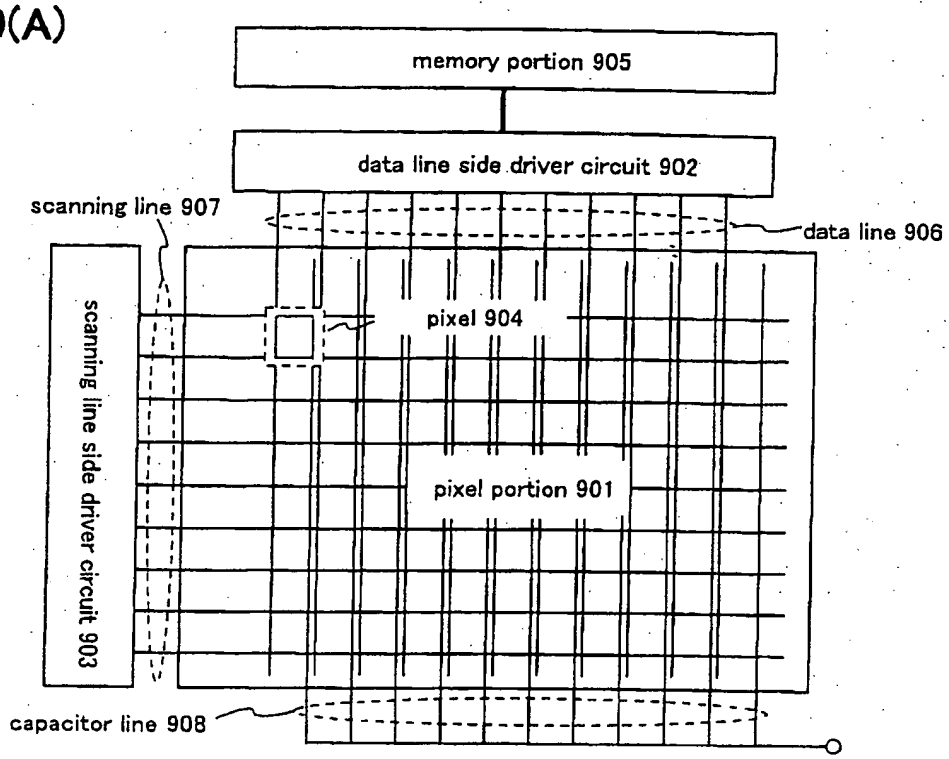
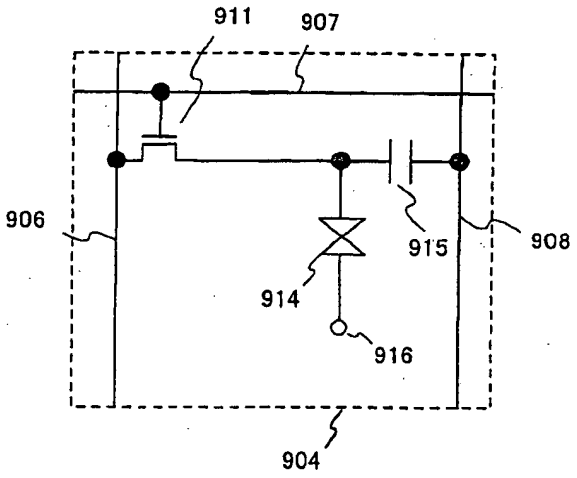


Fig. 9(B)



904 pixel 908 capacitor line 906 data line
907 scanning line 911 switching TFT
914 liquid crystal element 915 capacitor 916
counter electrode

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Fig. 10 (A)

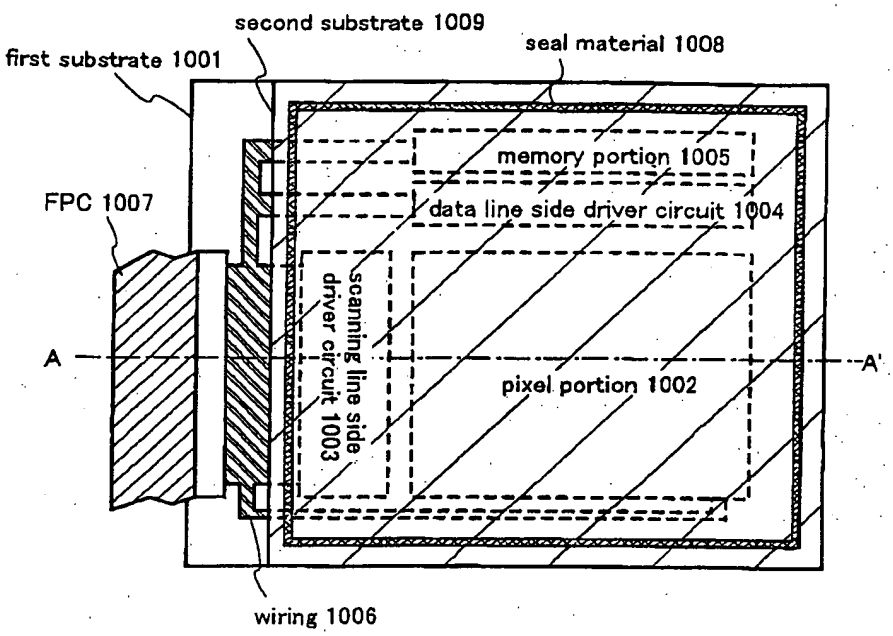


Fig. 10 (B)

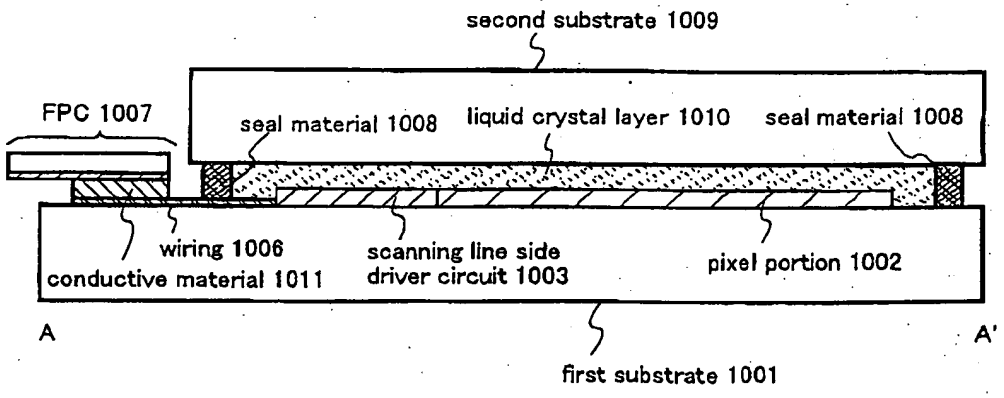
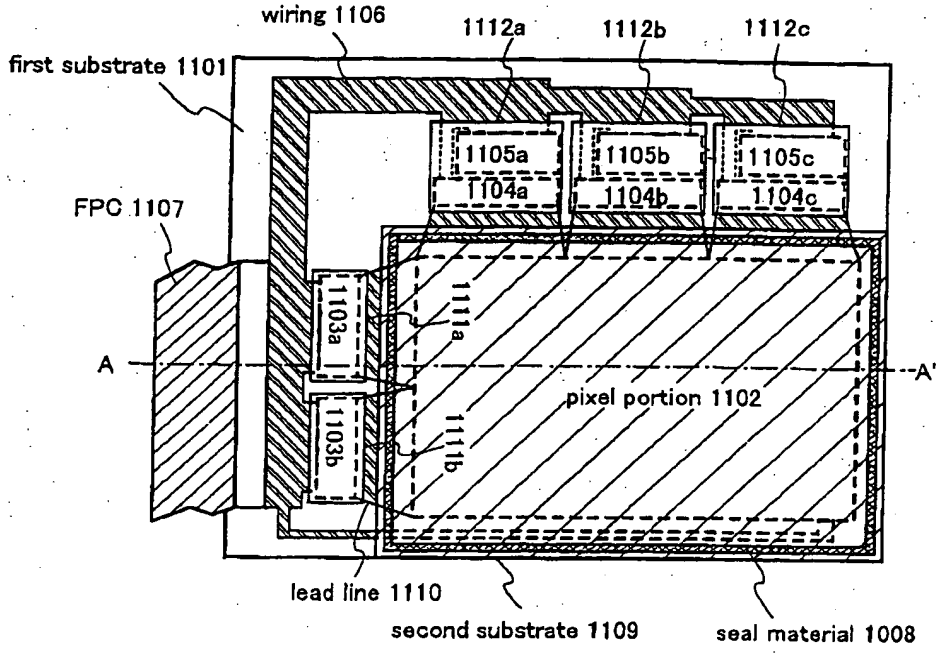


Fig. 11 (A)



1103a, 1103b scanning line side driver circuit
1104a, 1104b, 1104c data line side driver circuitc
1105a, 1105b, 1105c memory portion
1111a, 1111b scanning line side stick driver
1112a, 1112b, 1112c data line side stick driver

Fig. 11 (B)

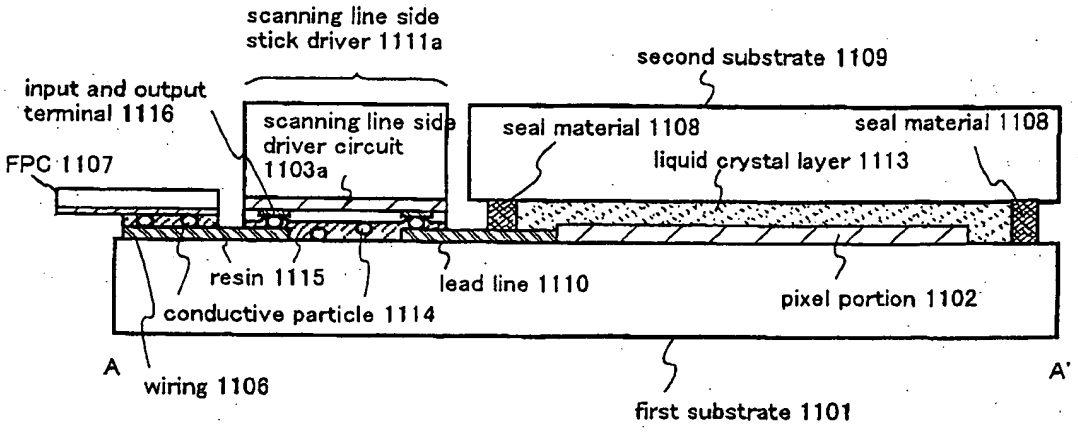


Fig. 12(A)

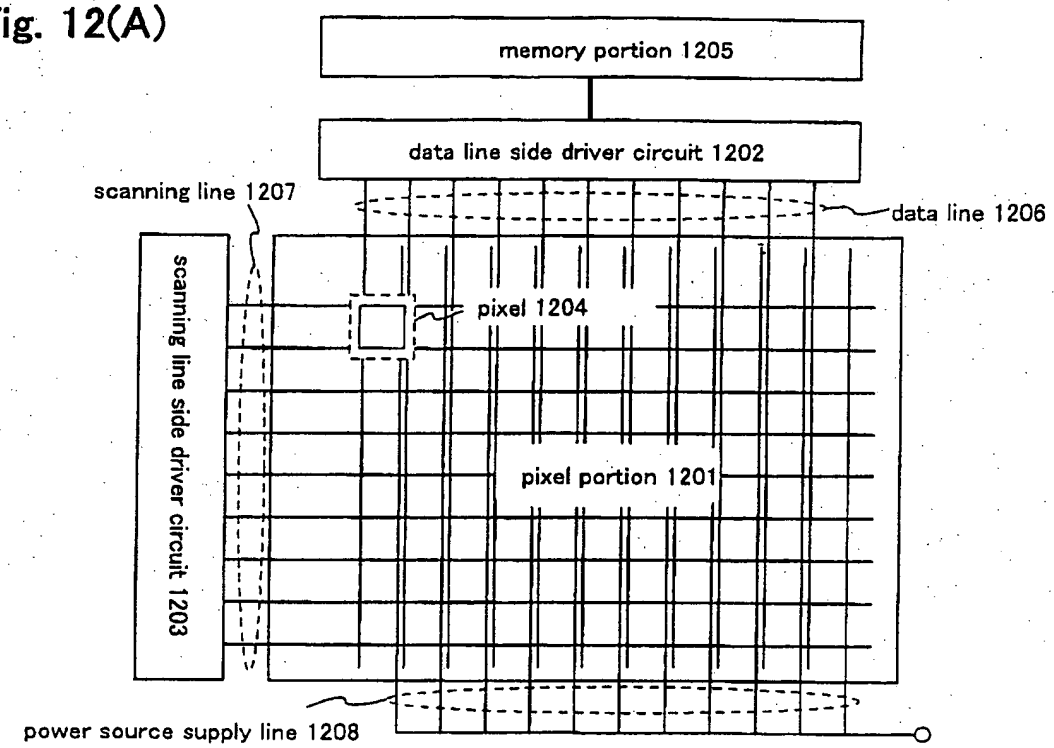
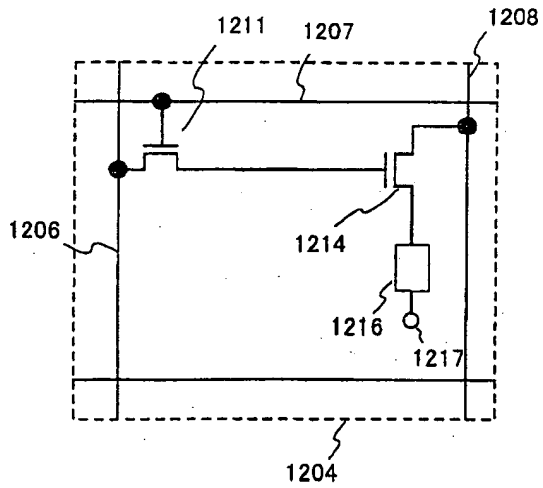


Fig. 12(B)



1204 pixel 1206 data line 1207 scanning line
1208 power source supply line 1211 switchin TFT
1214 EL driving TFT 1216 EL element 1217
counter electrode

Fig. 13(A)

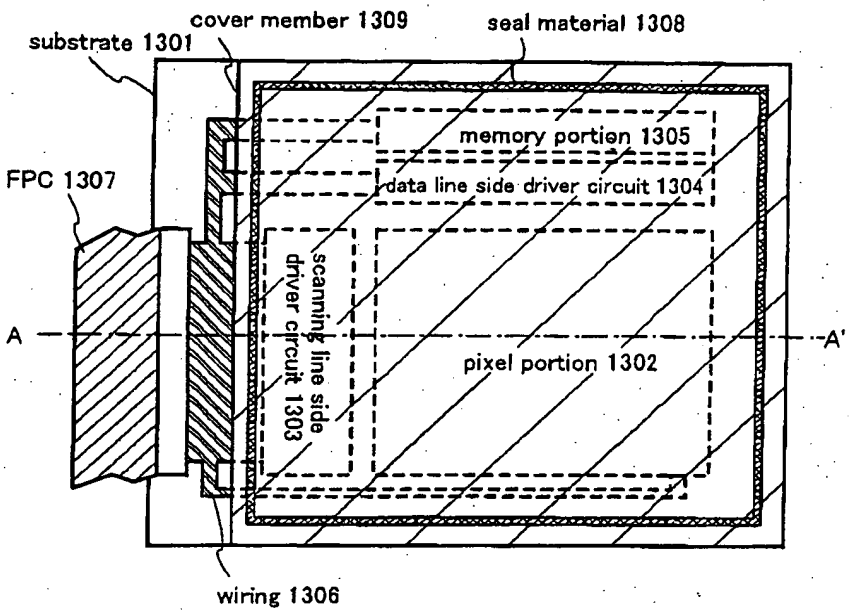


Fig. 13(B)

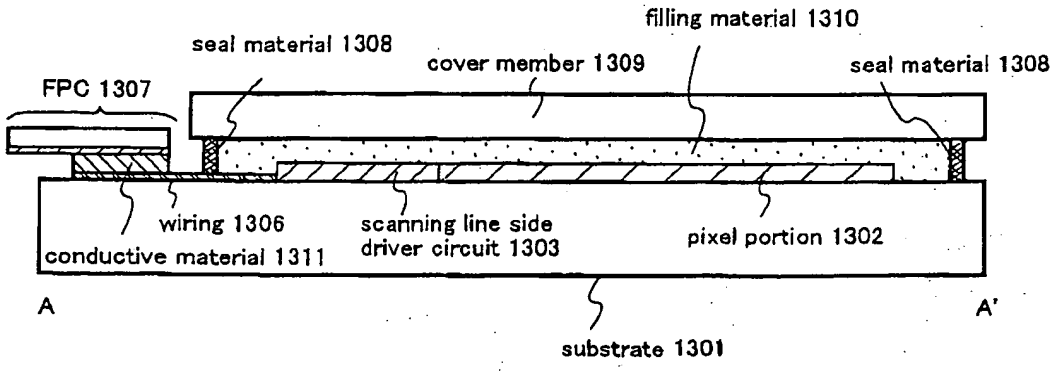
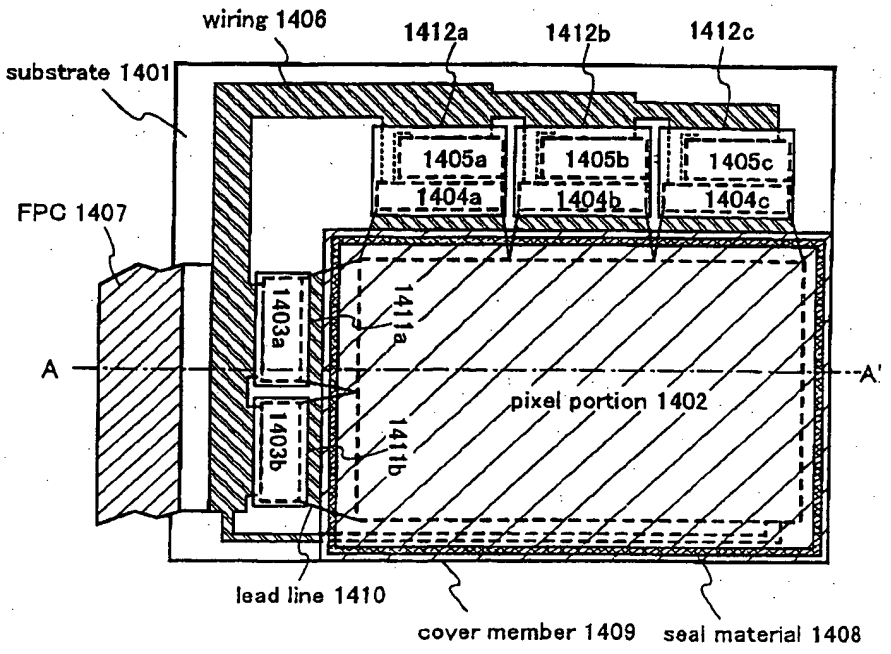


Fig. 14(A)



1403a, 1403b scanning line side driver circuit
1404a, 1404b, 1404c data line side driver circuit
1405a, 1405b, 1405c memory portion
1411a, 1411b scanning line side stick driver
1412a, 1412b, 1412c data line side stick driver

Fig. 14(B)

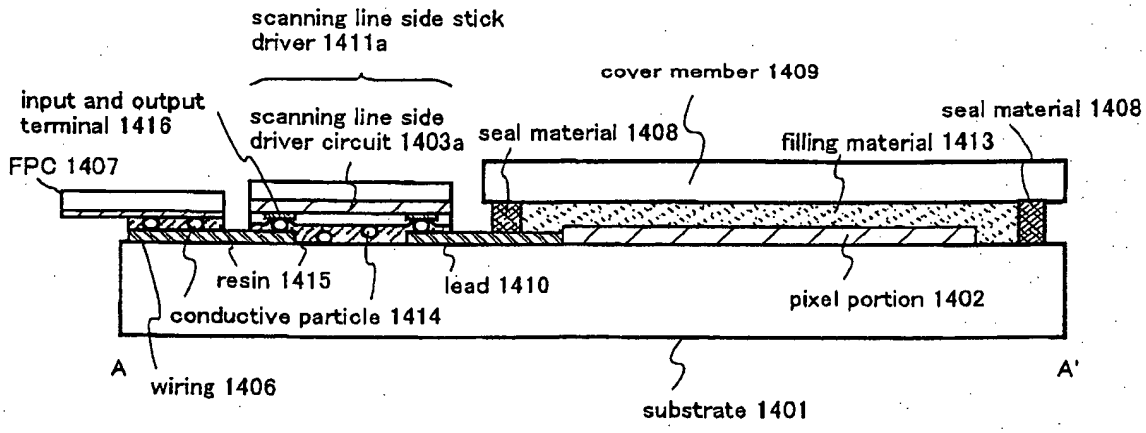


Fig. 15(A)

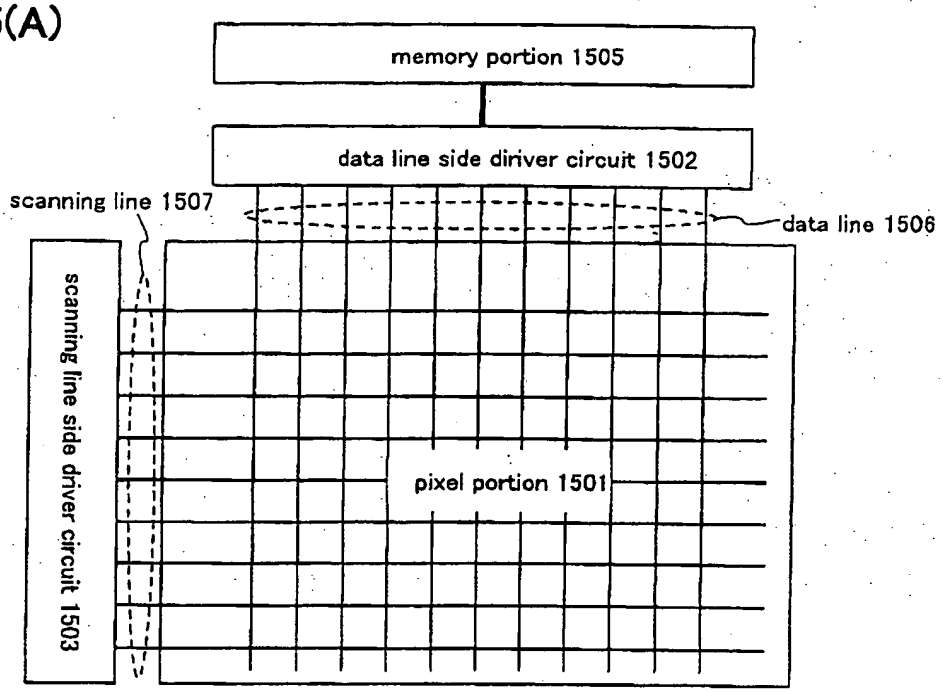
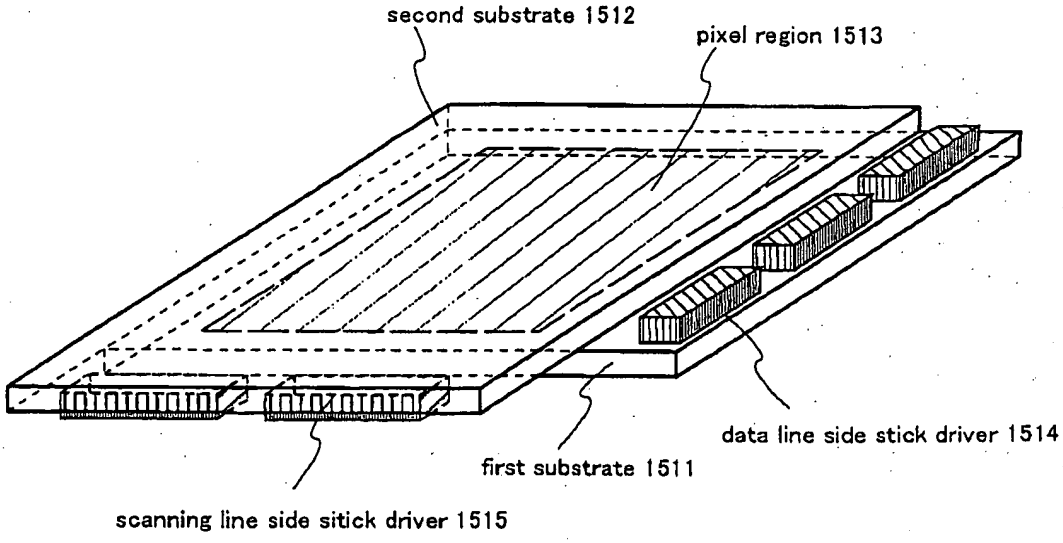


Fig. 15(B)



[Fig. 16]

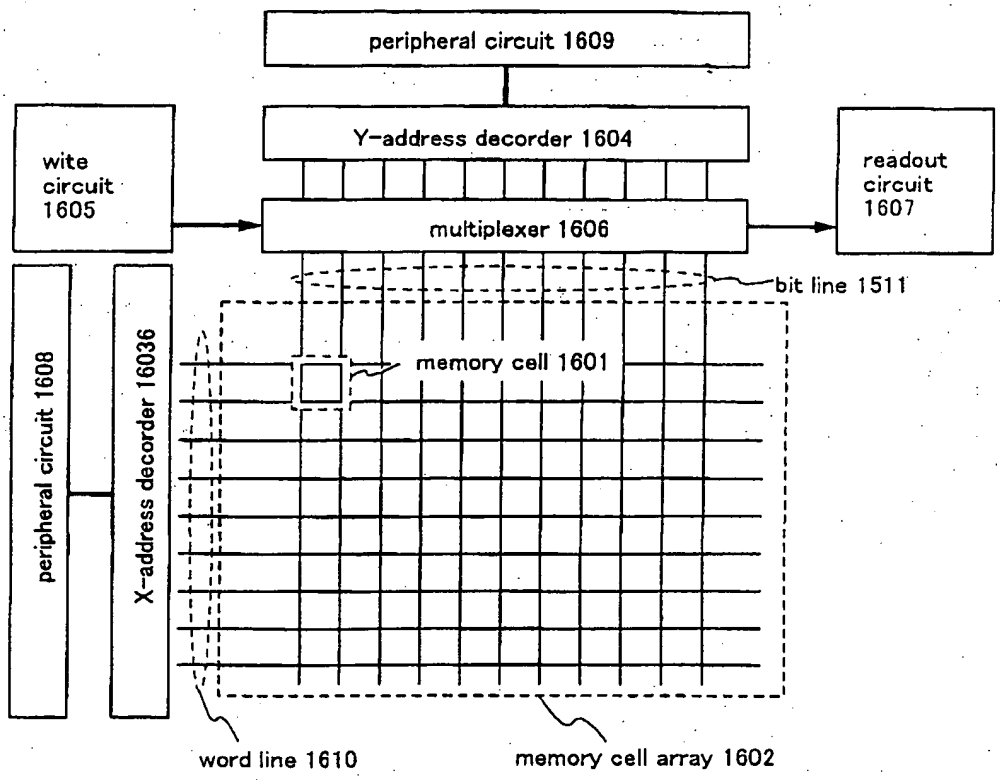

peripheral circuit 1609
Y-address decorder 1604
wite circuit 1605
multiplexer 1606
readout circuit 1607
bit line 1511
memory cell 1601
peripheral circuit 1608
X-address decorder 16036
word line 1610
memory cell array 1602

Fig. 17(A)

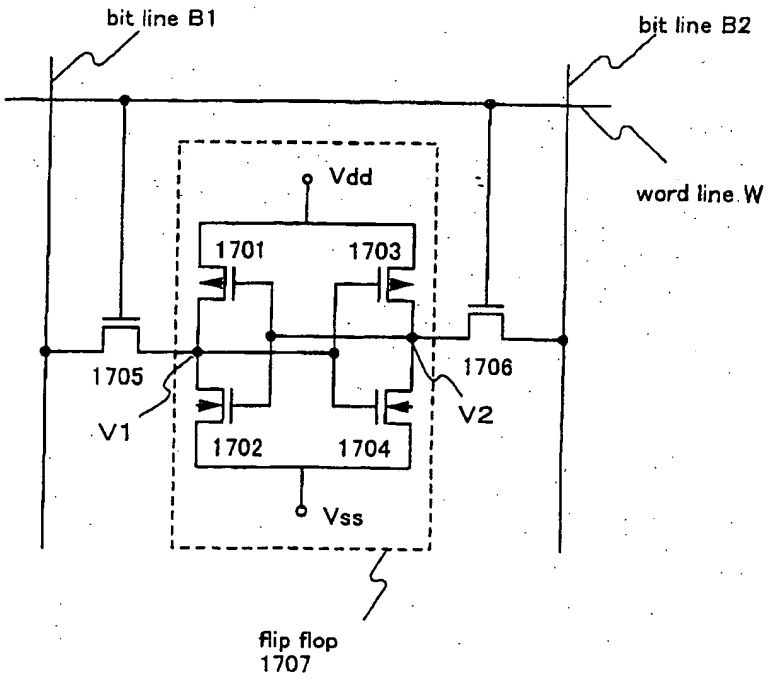
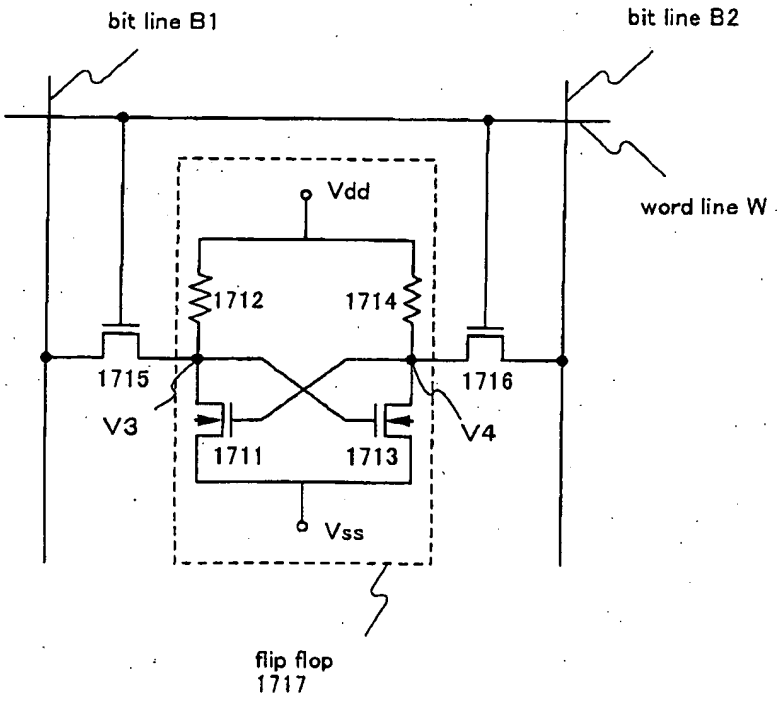
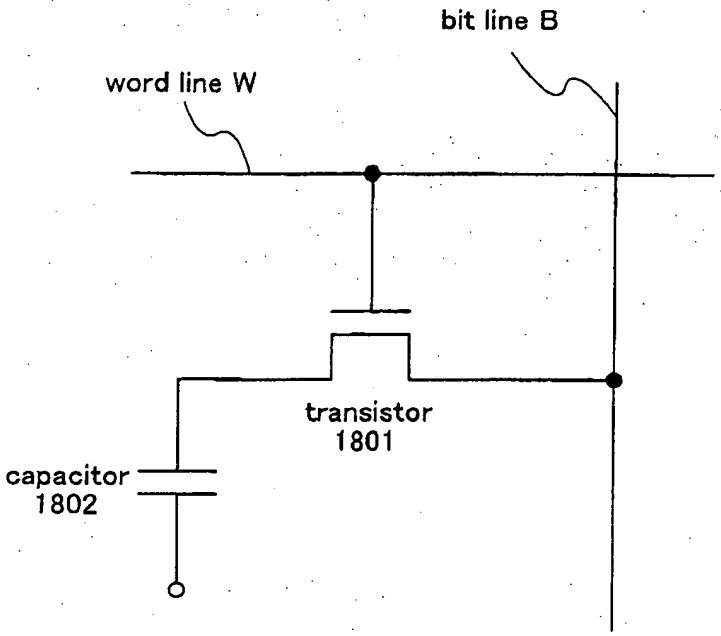


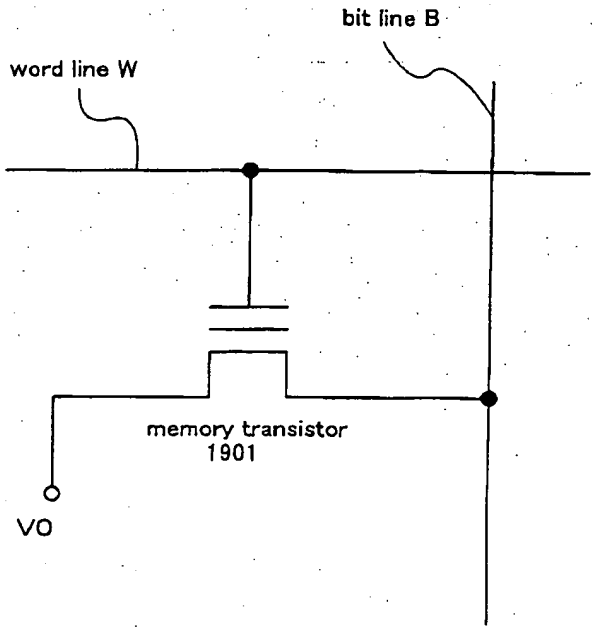
Fig. 17(B)



[Fig. 18]



[Fig. 19]



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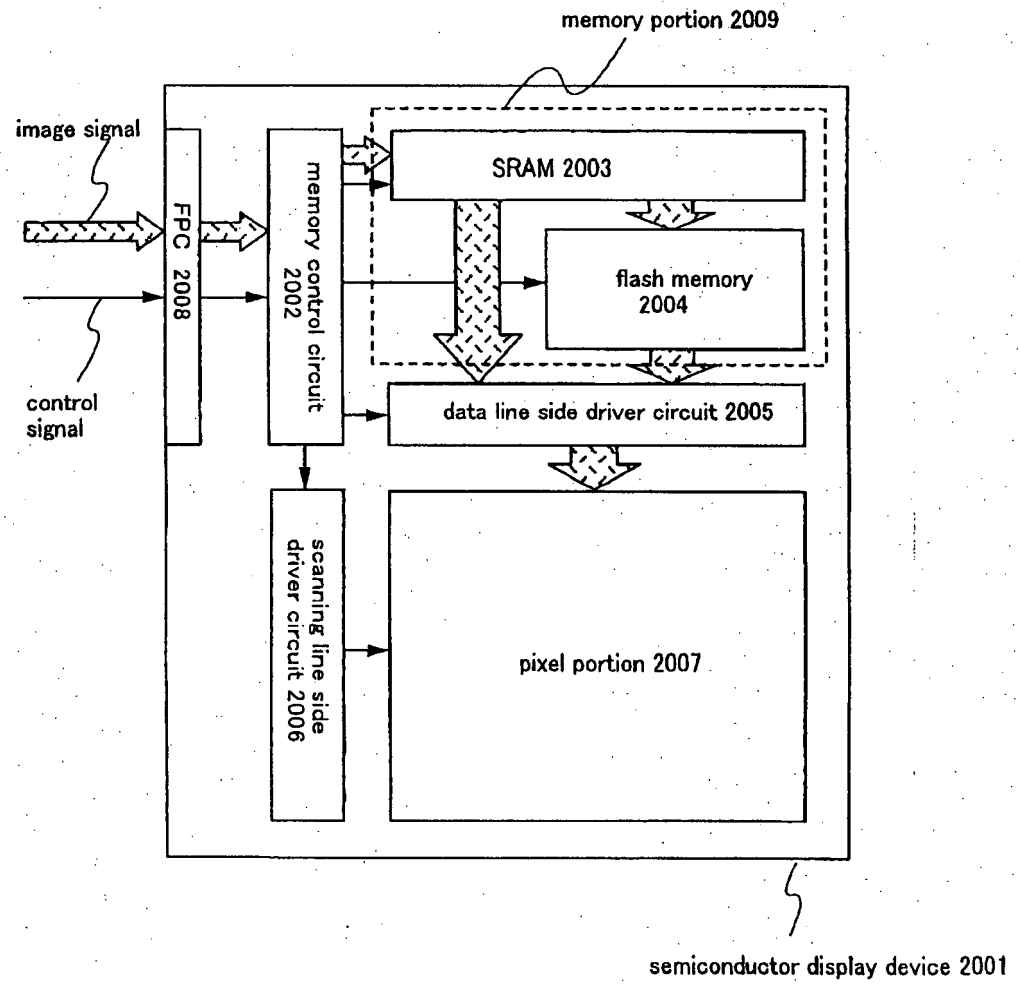
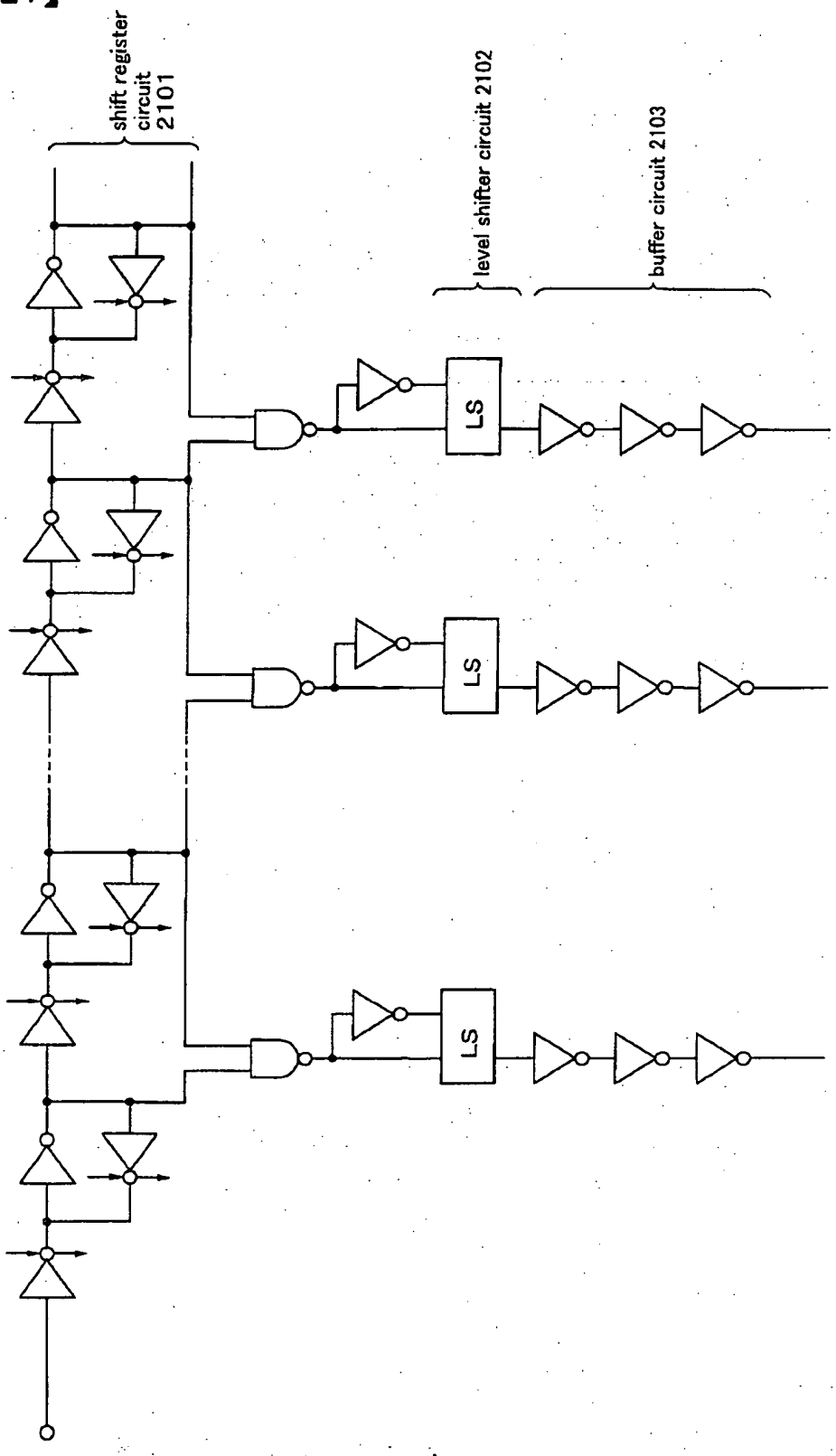
【Fig. 20】



【Fig. 21】


shift register circuit 2101
level shifter circuit 2102
buffer circuit 2103
LS
LS
LS

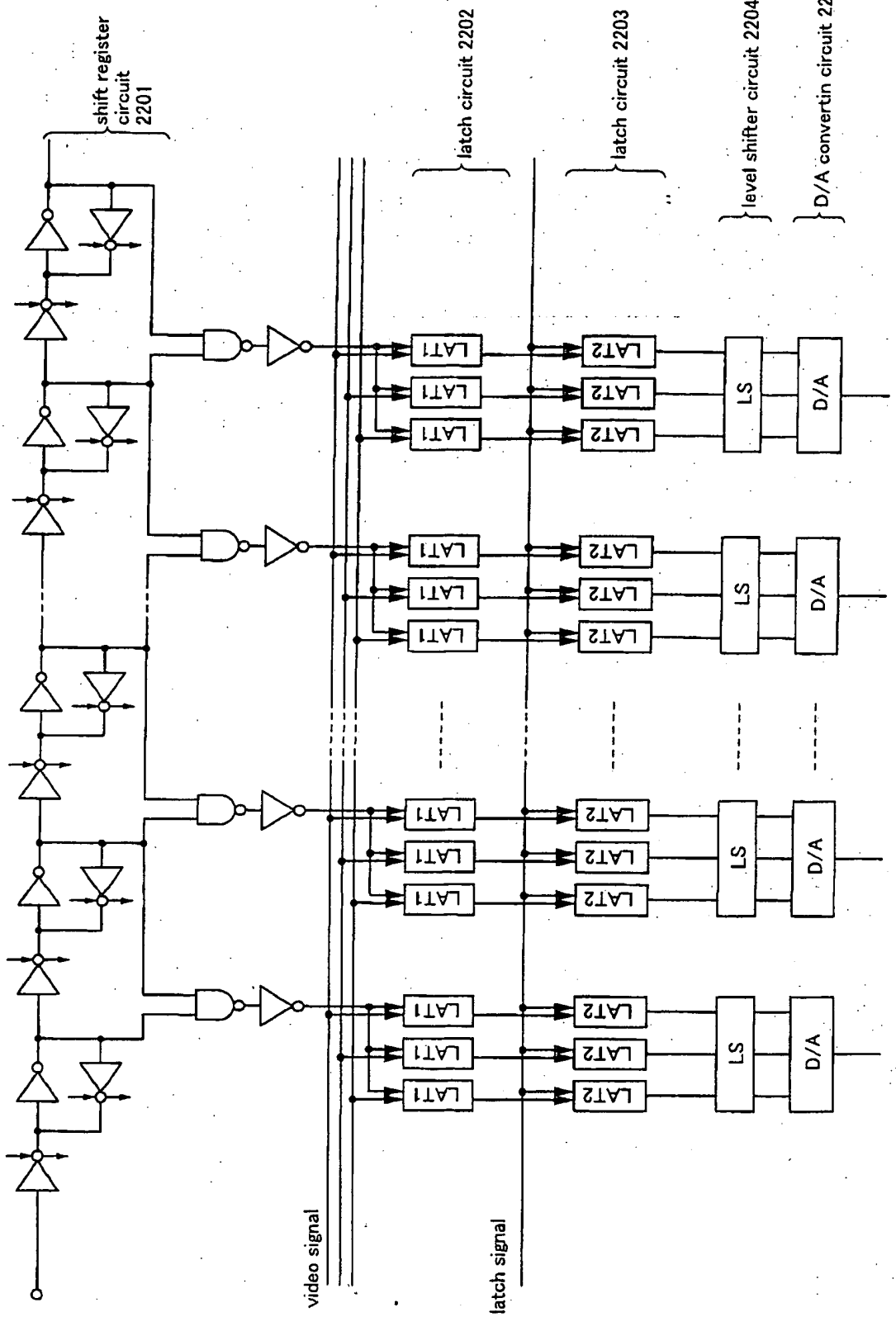

shift register circuit 2201
latch circuit 2202
latch circuit 2203
level shifter circuit 2204
D/A convertin circuit 2205
LAT1
LAT2
LS
D/A
video signal
latch signal

Fig. 22

JP2007-311860

Fig. 23(A) formation of island-like semiconductor layer, gate insulating film, and first and second conductive film for gate electrode

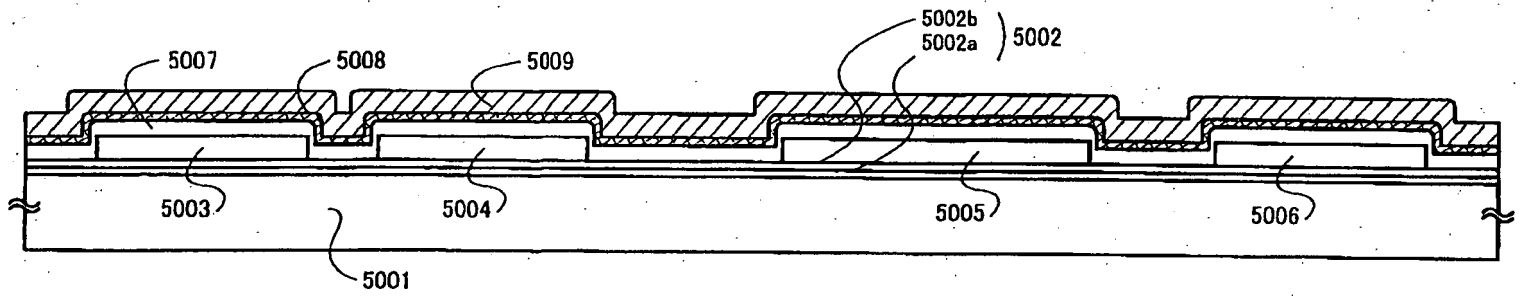


Fig. 23(B) first etching processing, first doping processing

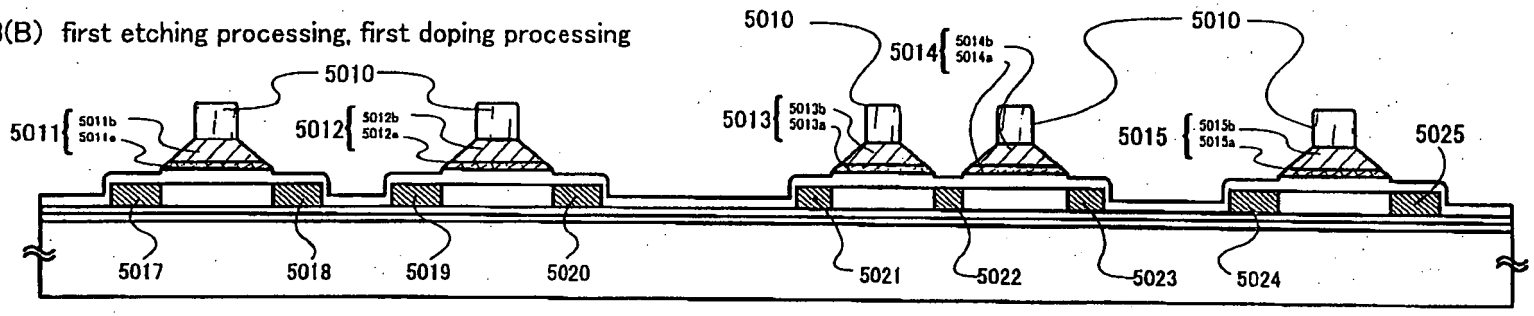
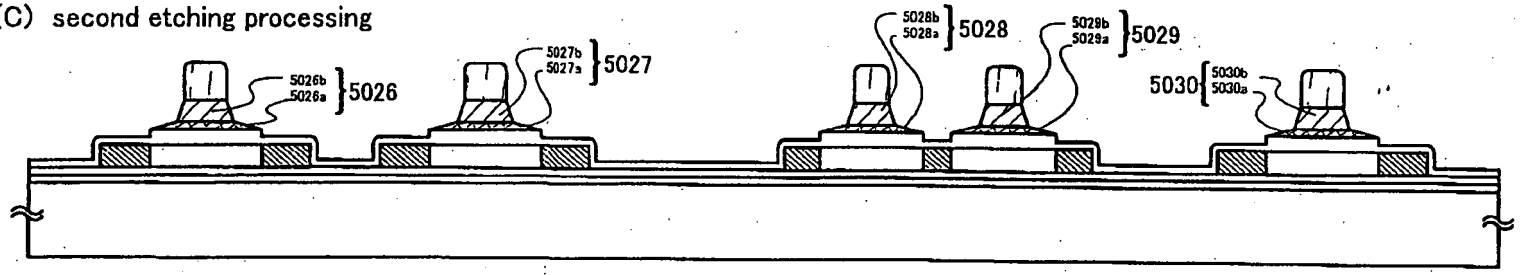


Fig. 23(C) second etching processing



5001 : substrate
5002 : base film
5003～5006 : semiconductor layer
5007 : gate insulating film
5008 : first conductive film
5009 : second conductive film
5010 : resist mask
5011～ 5015 : first shaped conductive layer
5011a～ 5015a : first conductive layer
5011b～ 5015b : second conductive layer
5017～ 5025 : first impurity region
5026～ 5030 : second shaped conductive layer
5026a～5030a : first conductive layer
5026b～5030b : second conductive layer

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Fig. 24(A) second doping processing

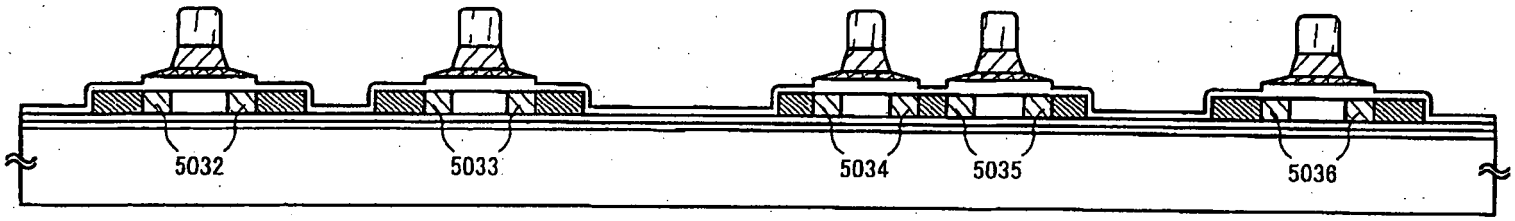


Fig. 24(B) third etching processing

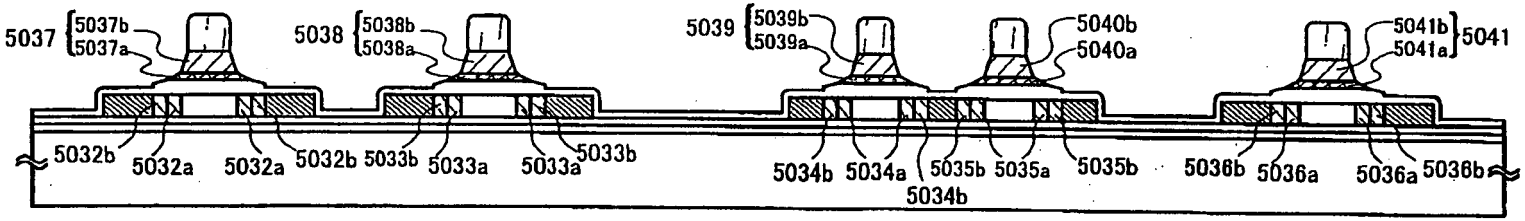
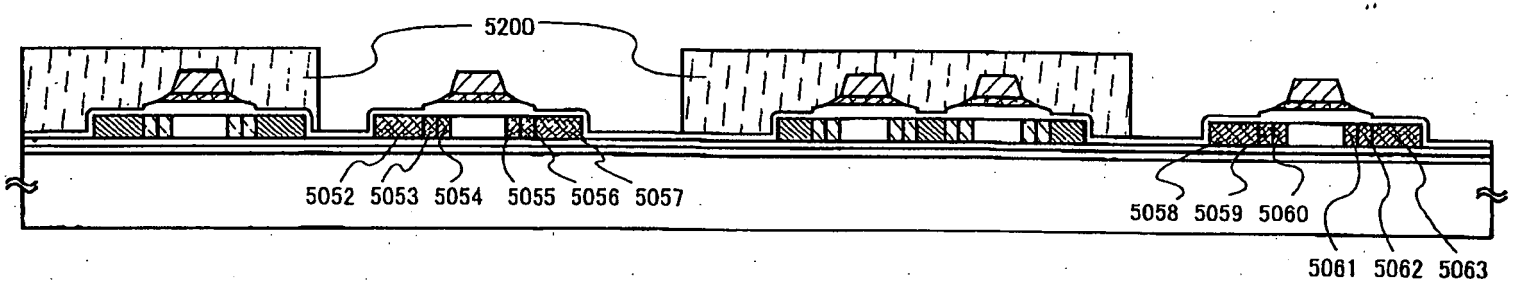


Fig. 24(C) third doping processing



5032～5036 : second impurity region
5032a～5036a : third impurity region
5032b～5036b : fourth impurity region

5037～5041 : third shaped conductive layer
5052～5063 : fifth impurity region
5200 : regist mask

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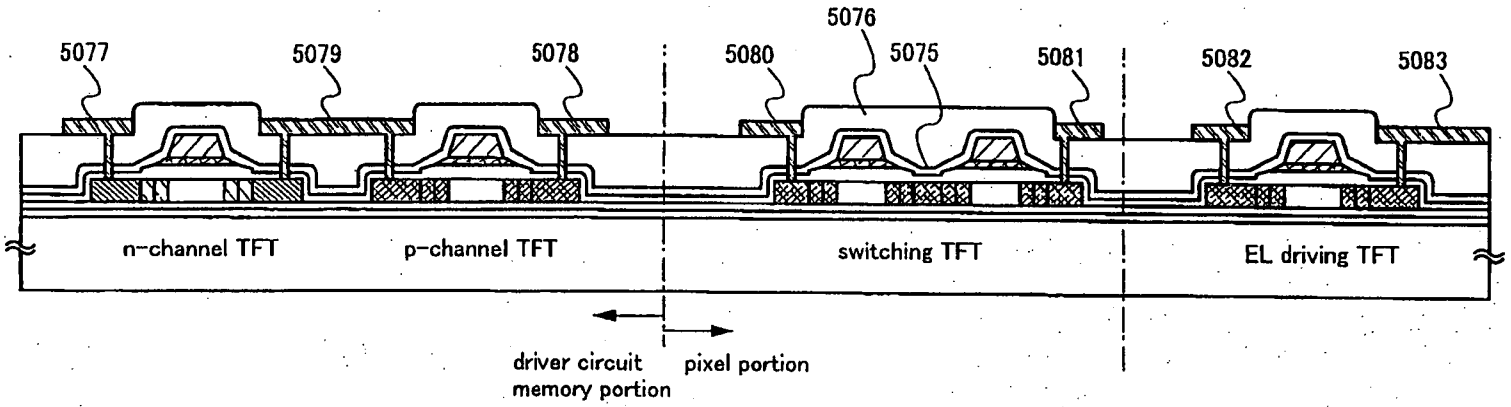
formation of first, second interlayer insulating films and wiring formation



5075 : first interlayer insulating film
5076 : second interlayer insulating film
5077～ 5083 : wiring

Fig. 25

P0000F-9676-0

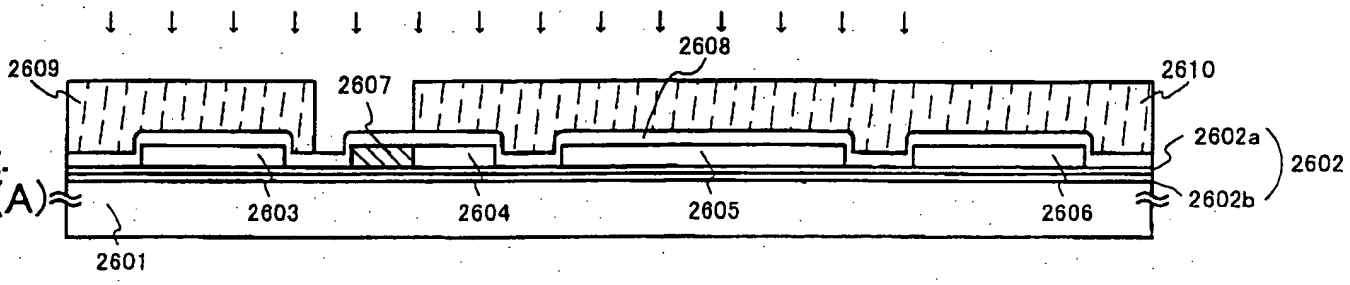


Fig. 26(A)

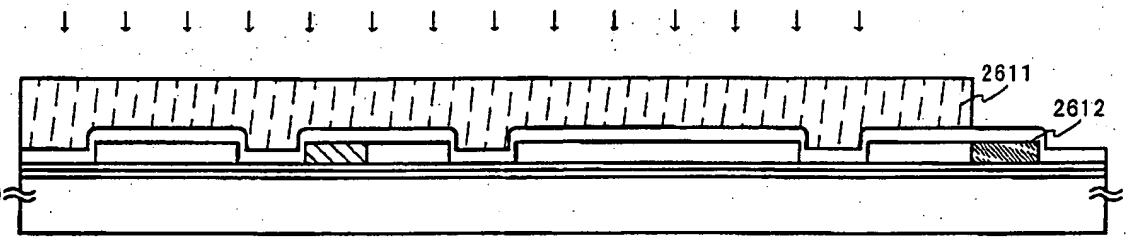


Fig. 26(B)

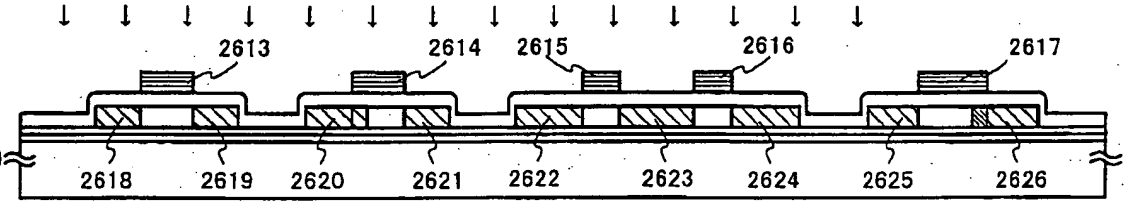


Fig. 26(C)

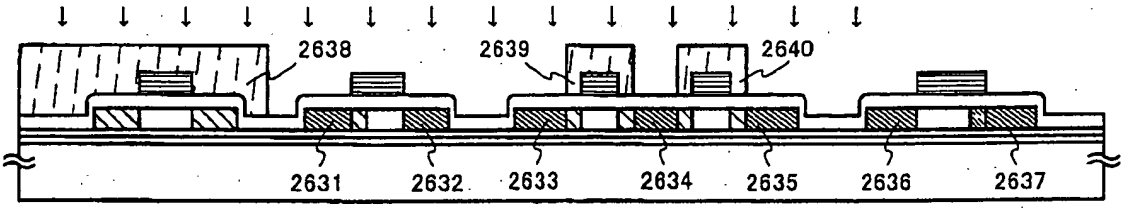


Fig. 26(D)

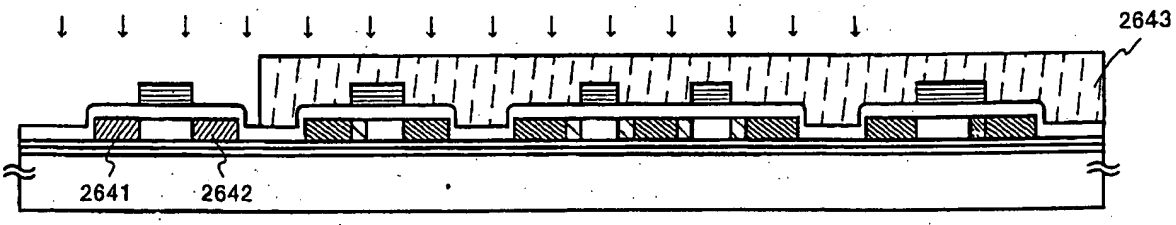


Fig. 26(E)

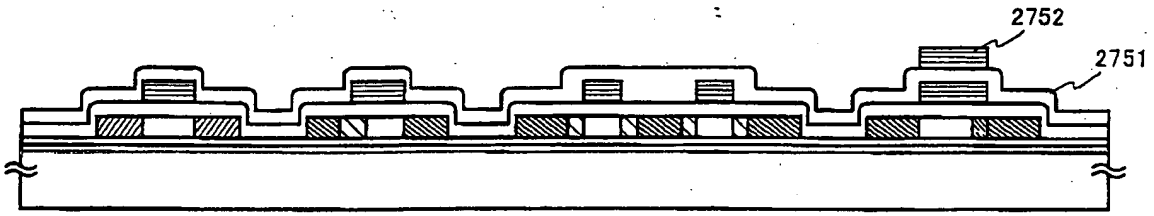


Fig.27(A)

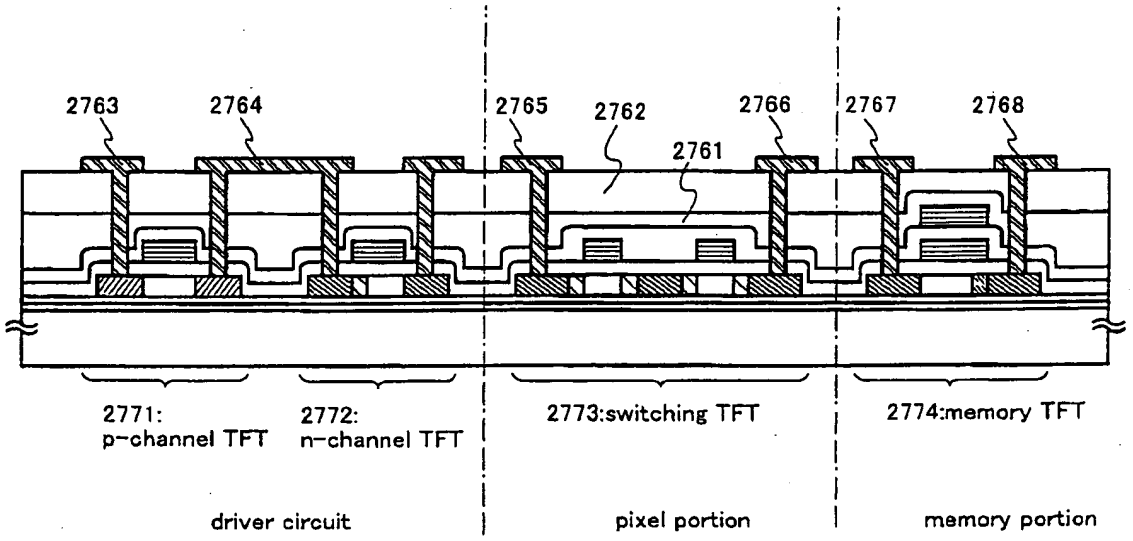


Fig.27(B)

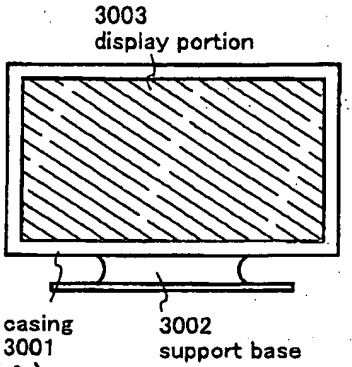


Fig. 28(A)

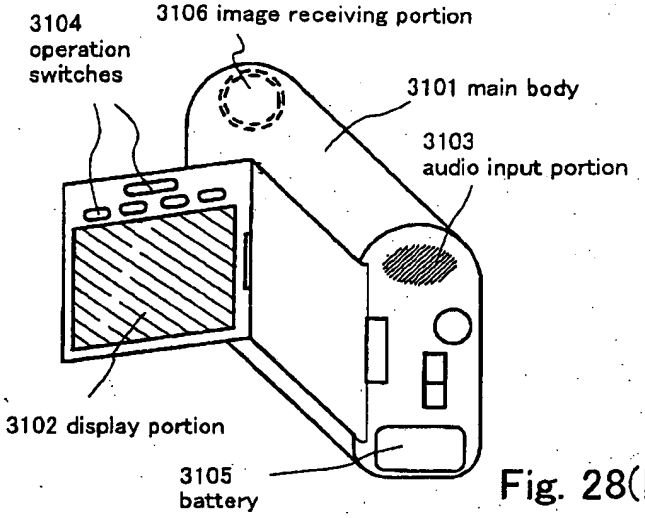


Fig. 28(B)

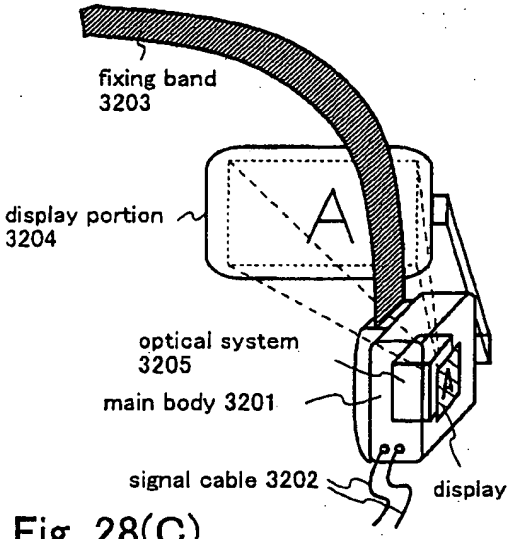


Fig. 28(C)

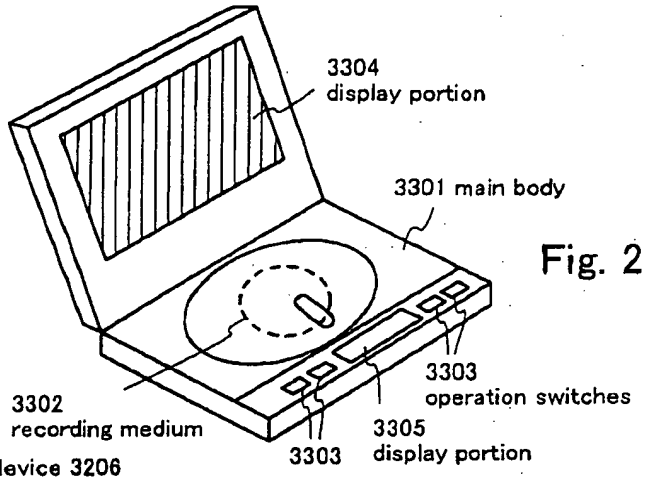


Fig. 28(D)

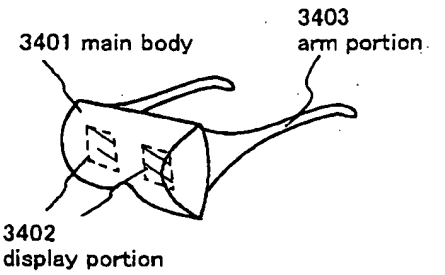


Fig. 28(E)

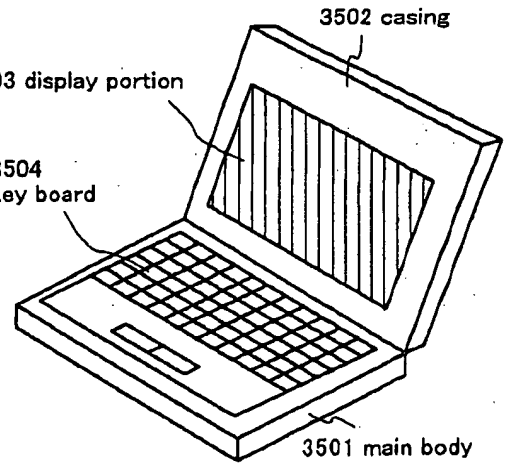


Fig. 28(F)

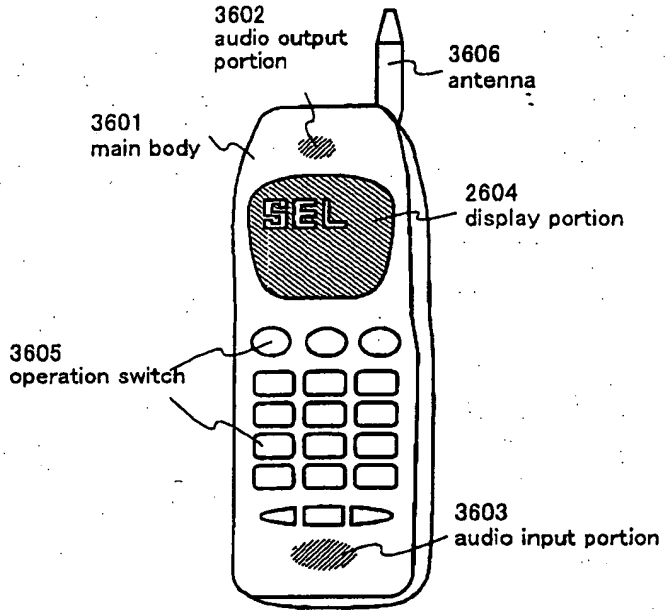


Fig. 29(A)

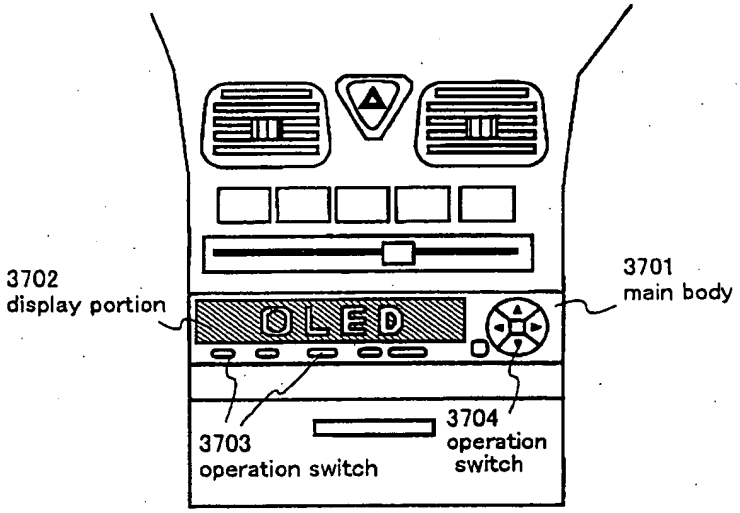


Fig. 29(B)